COUPLING OF SIGNALS BETWEEN ADJACENT FUNCTIONAL BLOCKS IN AN INTEGRATED CIRCUIT CHIP

ABSTRACT OF THE DISCLOSURE

[00150] A modifiable circuit for coupling at least two adjacent logic blocks in an integrated circuit chip is disclosed. The chip includes a plurality of metal layers and first and second power supply potentials. The circuit comprises a first and second metal interconnect structures, and an interconnect. The first metal interconnect structure traverses the plurality of metal layers using a first plurality of vias, wherein the first metal interconnect structure is located at a boundary of the at least two adjacent logic blocks. The second metal interconnect structure traverses the plurality of metal layers using a second plurality of vias, wherein the second metal interconnect structure is located at the boundary of the at least two adjacent logic blocks. The interconnect is formed between the at least two adjacent logic blocks by at least one of the first and second metal interconnect structures, wherein a state of the interconnect is programmable by altering any one of the plurality of metal layers or any one of a plurality of via layers.

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